Computer Organization and Architecture

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SUNRAISE INTERNATIONAL PUBLISHERS
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M/s SunRaise International Publishers

A Part of StudentsHelpline Publishing House (P) Ltd.

(An ISO 9001 : 2015 Certified Company)

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First Edition-2023

ISBN: 978-93-92311-00-0

Rs. 923/-

Printed at StudentsHelpline Group, S R Nagar, Hyderabad-38

Published by Surneni Mohan Naidu for SunRaise International Publishers, Hyderabad - 38

PREFACE

The First chapter deals with Introduction to Digital Electronics concepts, Logic Gates, Boolean Algebra, Flip Flops (SR, JK, D, T), Registers, Half Adder, Full Adder, Multiplexer, Demultiplexer, Decoder, and Encoder, introduction to block diagram of computer system and basic computer organization and architecture terminology discussion

The Second chapter deals with Register Transfer and Micro-operations: Register Transfer Language, Register Transfer, Bus and Memory Transfers – Three State Bus Buffers, Arithmetic Micro-Operations, Introduction to Binary Adder, Binary Adder-Subtractor, Binary Incrementer, Arithmetic Circuit, Logic Micro-Operations and Its Hardware Implementation, Shift Micro-Operations and Hardware Implementation, Arithmetic Logic Shift Unit. Introduction to Basic Computer Organization and Design in which deals with Instruction Codes, Stored Program Organization, Computer Registers, Common Bus System, Computer Instructions, Instruction Cycle, Memory Reference Instructions, Input Output and Interrupt.

The Third deals with Central Processing Unit, General Register Organization, Control Word, Stack Organization, Instruction Formats – Three Address, Two Address, One Address, Zero Address Instructions, Addressing Modes, Also includes Data Transfer And Manipulation, Arithmetic, Logical, Bit Manipulation, Program Control, Reduced Instruction Set Computer (RISC), CISC Characteristics.

Introduction to Micro programmed Control: Control Memory, Address Sequencing, Micro Program Example, Micro Program Sequencer.

The Fourth Chapter deals with Data Representation and discussed about conversions of various Number System and deals with Complements, Fixed point and Floating Representation ,and different binary codes representation and includes the study of Computer Arithmetic Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations.

Chapter Fifth deals with Input-Output Organization: Input Output Interface, I/O Bus and Interface Modules, I/O Vs Memory Bus, Isolated Vs Memory Mapped I/O. Methods Introduction to Asynchronous Data Transfer, Handshaking, Programmed I/O, Interrupt-Initiated I/O**,** Priority Interrupt – Daisy Chaining, Parallel Priority, Priority Encoder, Interrupt Cycle, DMA Controller And Transfer.

The sixth chapter includes the study of Pipeline and Vector Processing, Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor. And also deals with Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Interprocessor arbitration, Interprocessor communication and synchronization, Cache Coherence. RAM Chip, ROM Chips, Memory Address Map, Associative Memory, Cache Memory, Virtual Memory.

ACKNOWLEDGEMENT

At first, we would like to thank the Principal and Management of St. Martin's Engineering College for their tremendous support and direction for preparing this text book. Preparation and publication of this book would not have been possible without their support. We are especially indebted to Sri M. Laxman Reddy Garu, Chairman of the College and **Sri G. Chandrasekhar Yadav Garu,** Executive Director of the college.

All our authors are specially thankful to our beloved Principal Dr. P. Santosh Kumar Patra who had been supportive of our career goals and who worked actively to provide us all the facilities to pursue our goals. We would also like to thank **Dr. M. Narayanan,** Head of the Department of Computer Science and Engineering, for his suggestions, support and encouragement that helped us in the improvement of this book. We express our gratitude to our family members and to our colleagues for their continuous support and encouragement.

The text contained in this book has been used by us a number of times in preparing handouts,tutorial sheets, home assignments, class tests, technical quiz questions, viva-voce tests, remedial study material, self-learning packages for enhancing individual learning etc. over the years. The feedback received from students and teachers have been used to refine the text.

We would, therefore, like to acknowledge the contribution made by our students and by all those teachers who read this text and provided feedback for improvement. Since this revision work wascarried out over as considerable period of time, we find it difficult to list the names of students whomade direct or indirect contribution while final content of this book.

Authors would like to acknowledge the curriculum development experts engaged by the AICTE in developing the syllabus for this subject, who we find is a well-balanced one and incorporates the important topics of Constitution of India for Engineering/Technology students.

Finally, we would like to express our sincere appreciation to all the team members of **M/s SunRaise International Publishers,** who have contributed to the publication of this book

Computer Organization and Architecture

COURSE OUTCOMES

Upon successful completion of the course, the student is able to

1. Understand the basics of instructions sets and their impact on processor design.
2. Demonstrate an understanding of the design of the functional units of a digital computer system.
3. Evaluate cost performance and design trade-offs in designing and constructing a computer processor including memory.
4. Design a pipeline for consistent execution of instructions with minimum hazards.
5. Recognize and manipulate representations of numbers stored in digital computers

Unit-I: Basic Operations

Digital Computers: Introduction, Block diagram of Digital Computer, Definition of ComputerOrganization, Computer Design and Computer Architecture.

Register Transfer Language and Micro operations: Register Transfer language, Register Transfer,Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations,Arithmetic logic shift unit.

Basic Computer Organization and Design: Instruction codes, Computer Registers Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

Unit-II: CPU & Micro Programmed Control

Microprogrammed Control: Control memory, Address sequencing, micro program example, designof control unit.

Central Processing Unit: General Register Organization, Instruction Formats, Addressing modes,Data Transfer and Manipulation, Program Control.

Unit-III: Data Representation and Computer Artihmetic

Data Representation: Data types, Complements, Fixed Point Representation, Floating Point Representation.

Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Division Algorithms,Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

Unit-IV: Input-output and Memory Organization

Input-Output Organization: Input-Output Interface, Asynchronous data transfer, Modes of Transfer,Priority Interrupt Direct memory Access.

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory,Cache Memory.

Unit-V: Pipeline Processing and Multi Processors

Reduced Instruction Set Computer: CISC Characteristics, RISC Characteristics.

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, InstructionPipeline, RISC Pipeline, Vector Processing, Array Processor.

Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Interprocess or arbitration, Interprocessor communication and synchronization, Cache Coherence.